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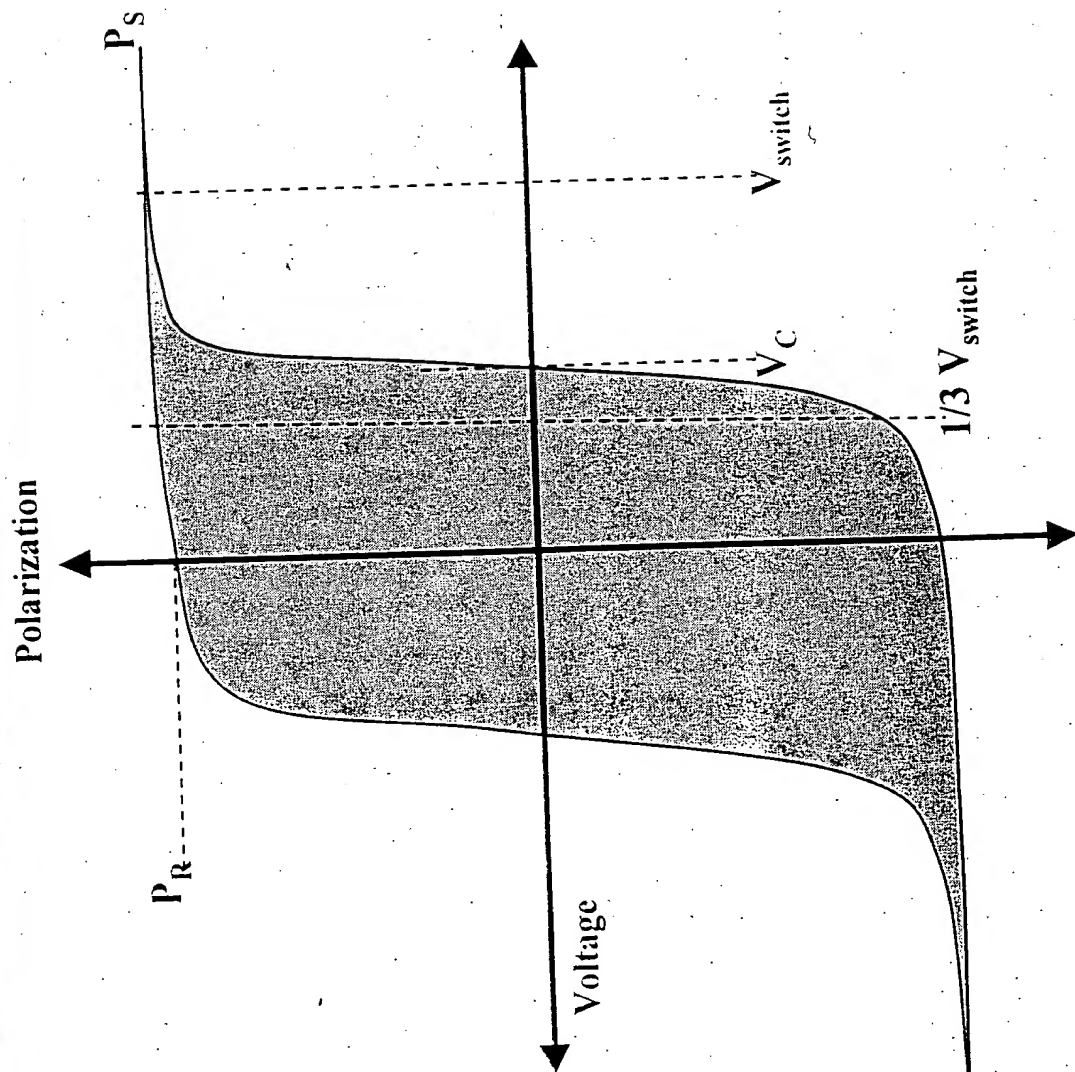


Fig.1

FIG. 2

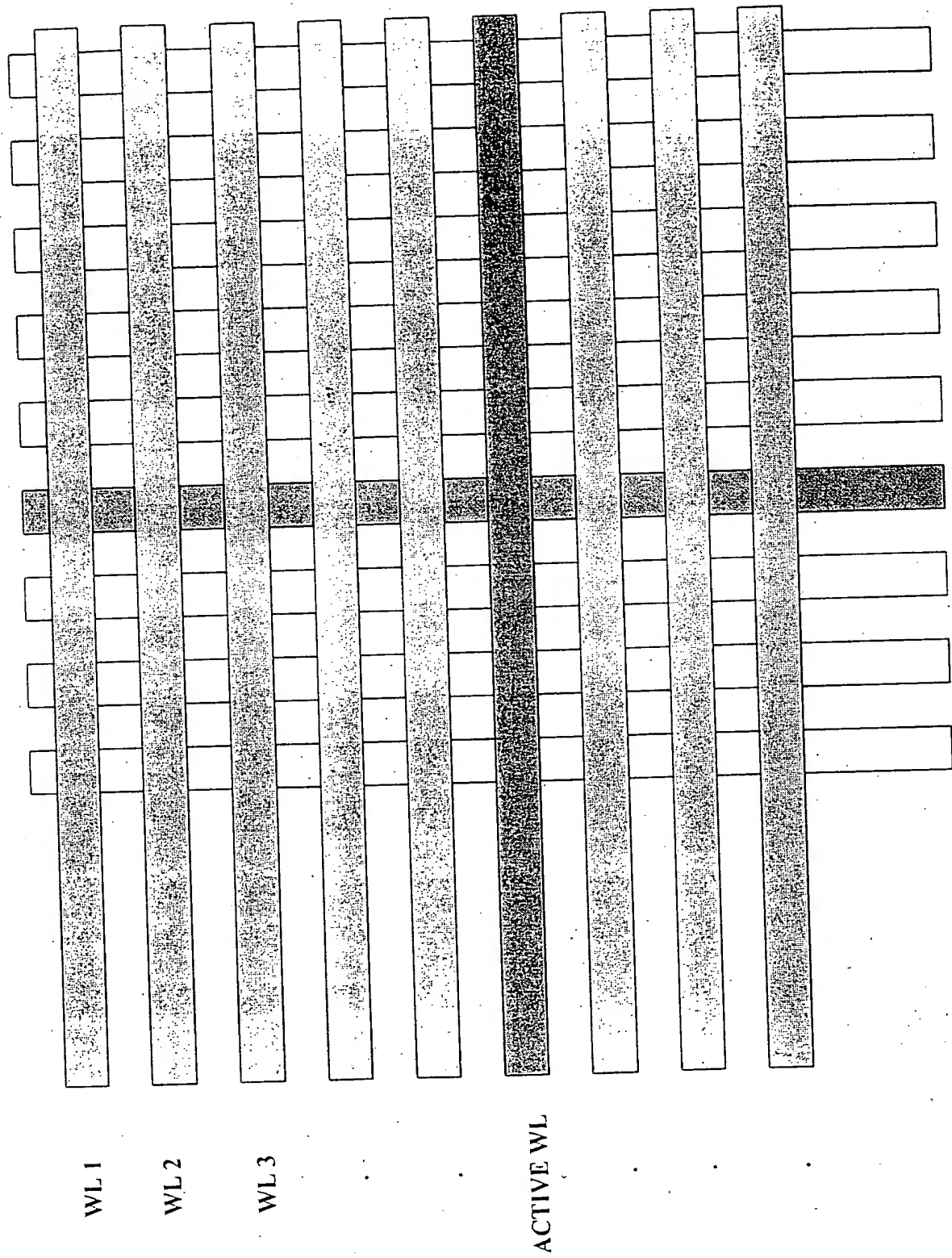


FIG.2

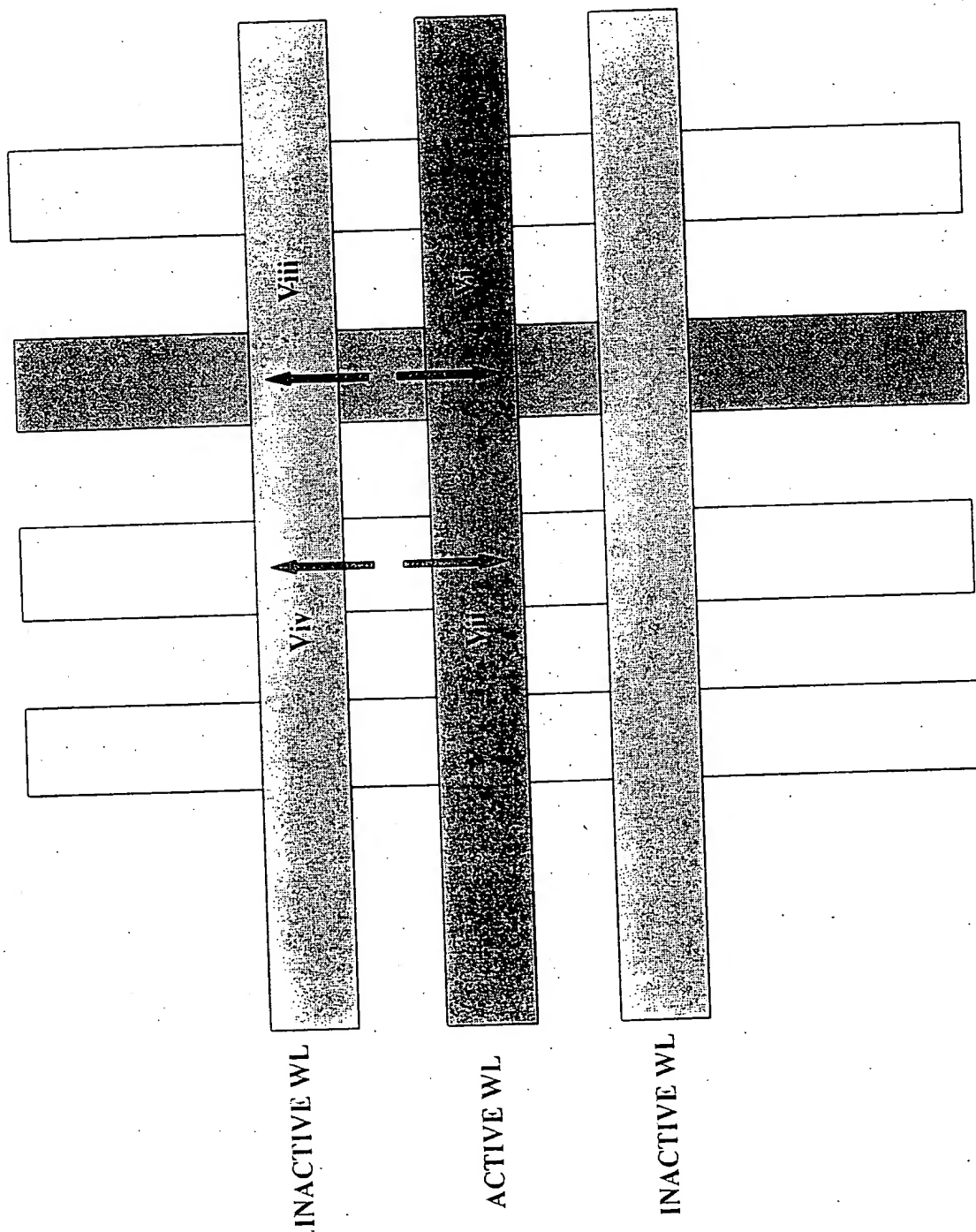
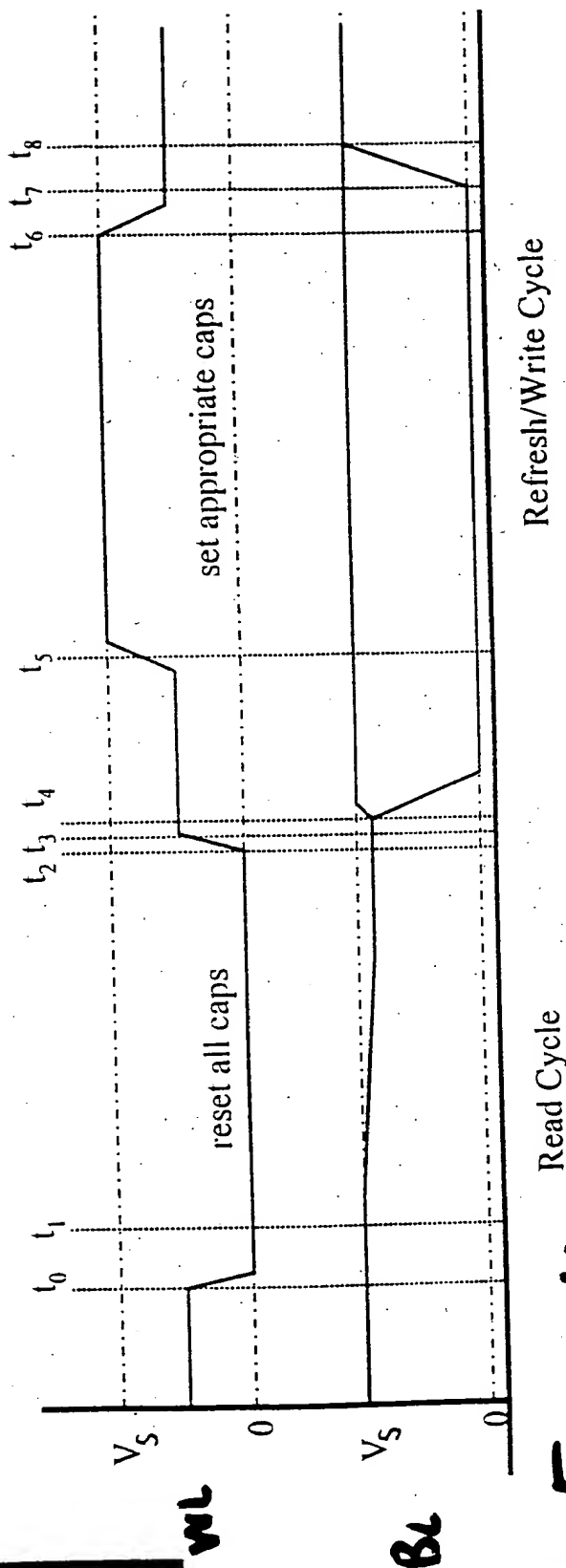
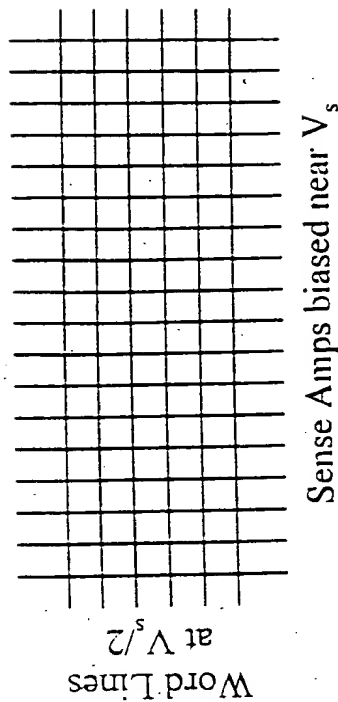


FIG.3

3 Level Passive Matrix Switching Protocol

Maximum depolarizing voltage $V_s/2$

- t_0 : word line latched, active pulldown to 0
- t_1 : bit line clamp released - sense amp on
- t_2 : bit line decision - data latched
- t_3 : word line returned to quiescent $V_s/2$
- t_4 : write data latched on bit lines
- t_5 : word line pulled to V_s - set/reset caps
- t_6 : word line returned to quiescent $V_s/2$
- t_7 : bit lines actively returned to V_s clamp
- t_8 : read/write cycle complete



Read Cycle

Refresh/Write Cycle

Fig. 4

3 Level Passive Matrix Switching Protocol

- t_0 : word line latched, active pull μp to V_s
- t_1 : bit line clamp released - sense amp on
- t_2 : bit line decision - data latched
- t_3 : word line returned to quiescent $V_s/2$
- t_4 : write data latched on bit lines
- t_5 : word line pulled to 0 - set/reset caps
- t_6 : word line returned to quiescent $V_s/2$
- t_7 : bit lines actively returned to 0 clamp
- t_8 : read/write cycle complete

Maximum depolarizing voltage $V_s/2$

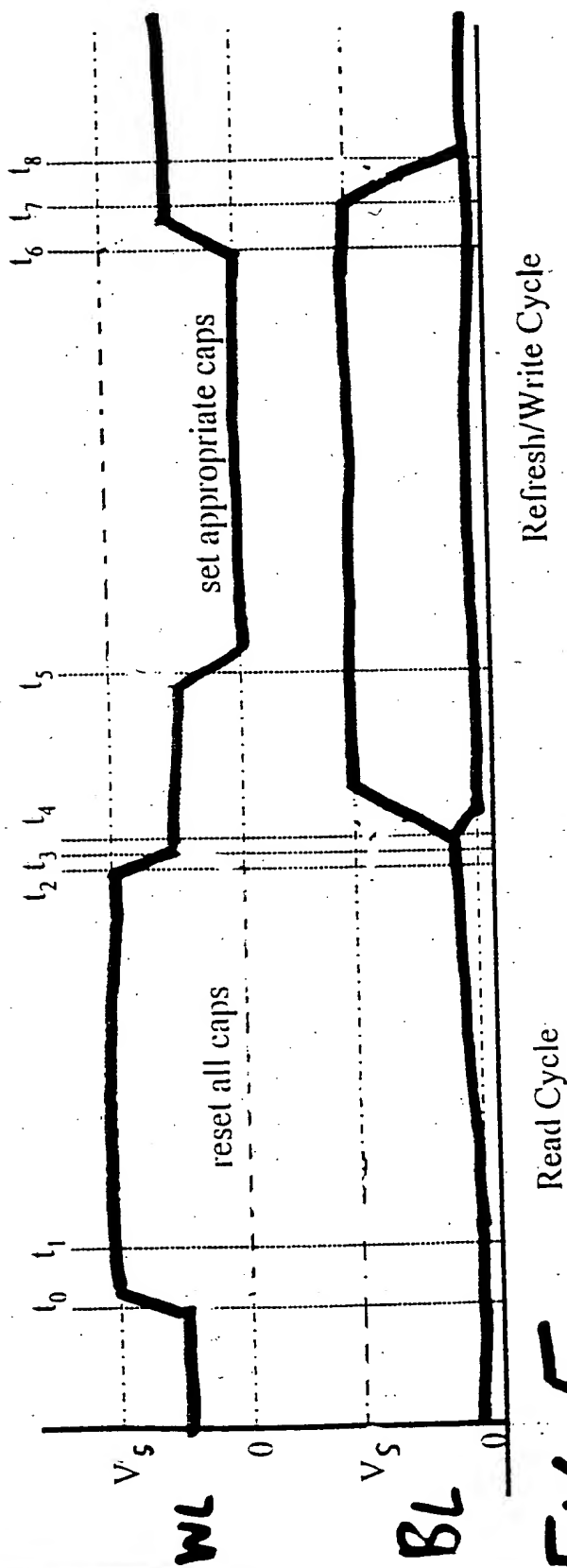
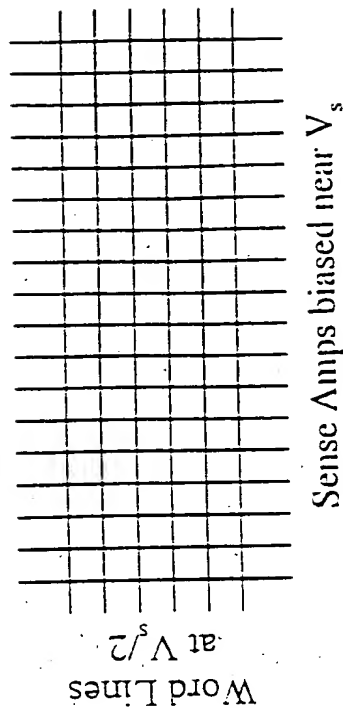


FIG. 5

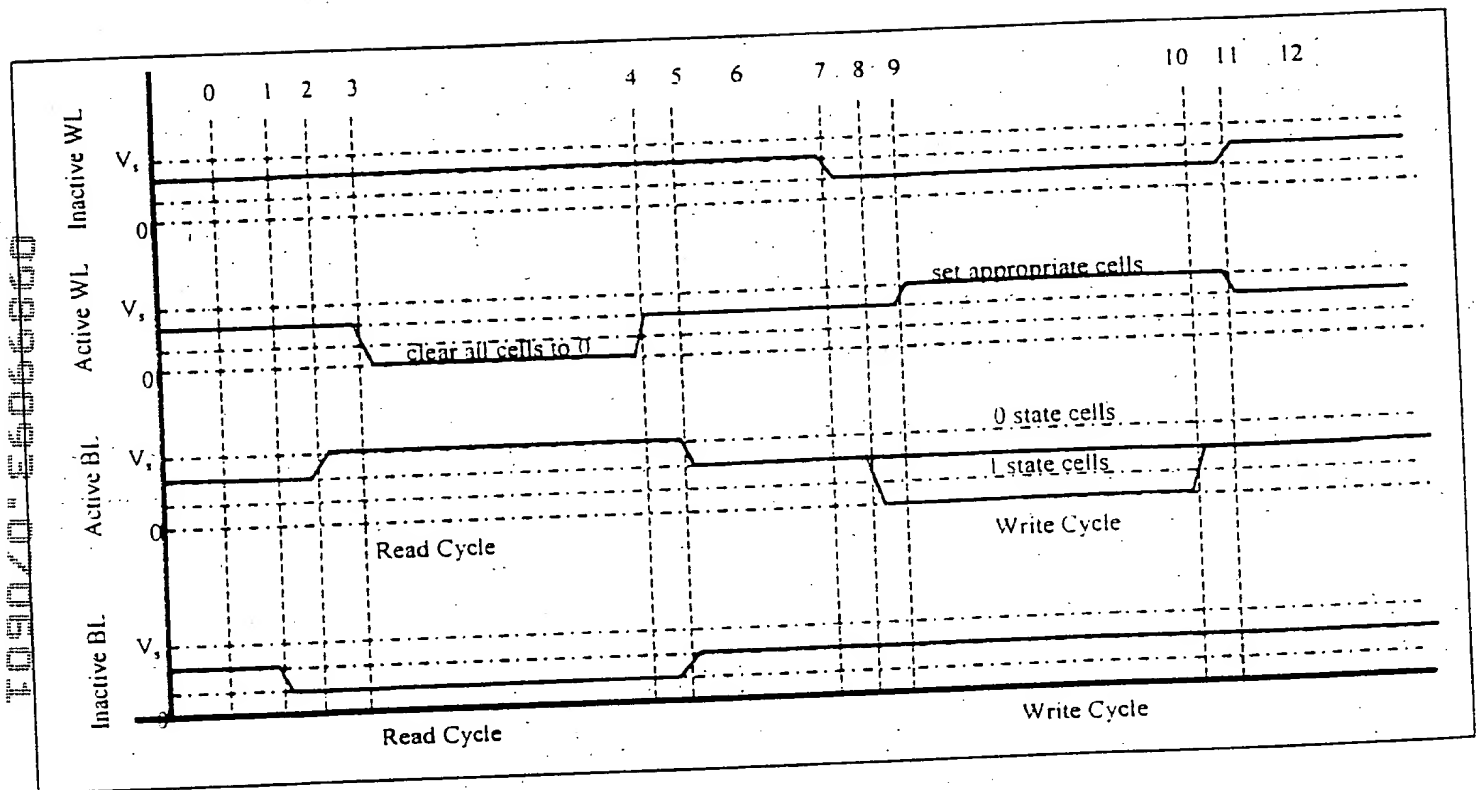


FIG. 6.

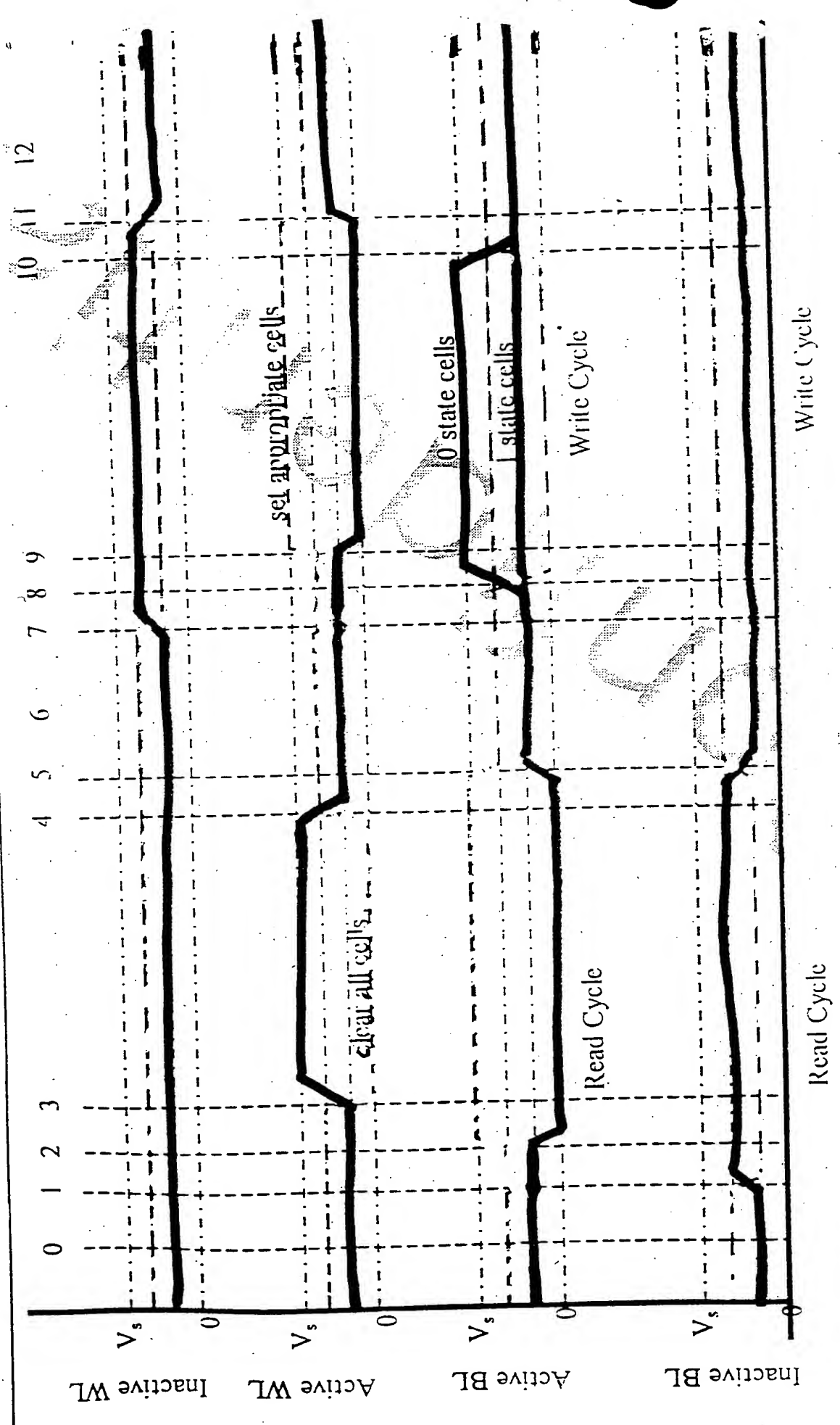


FIG. 7

Five Level Timing Diagram

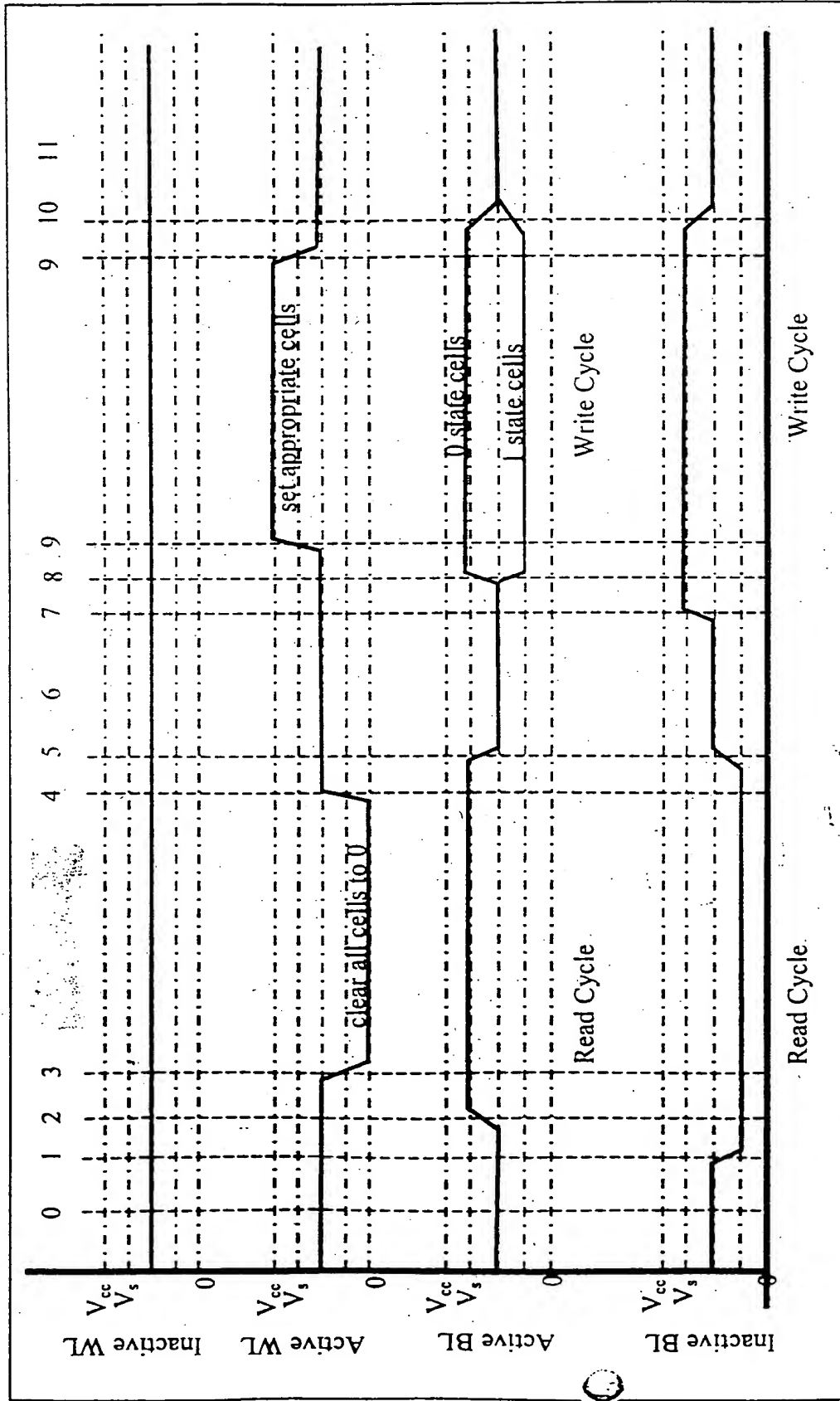


FIG. 8

Five Level Timing Diagram

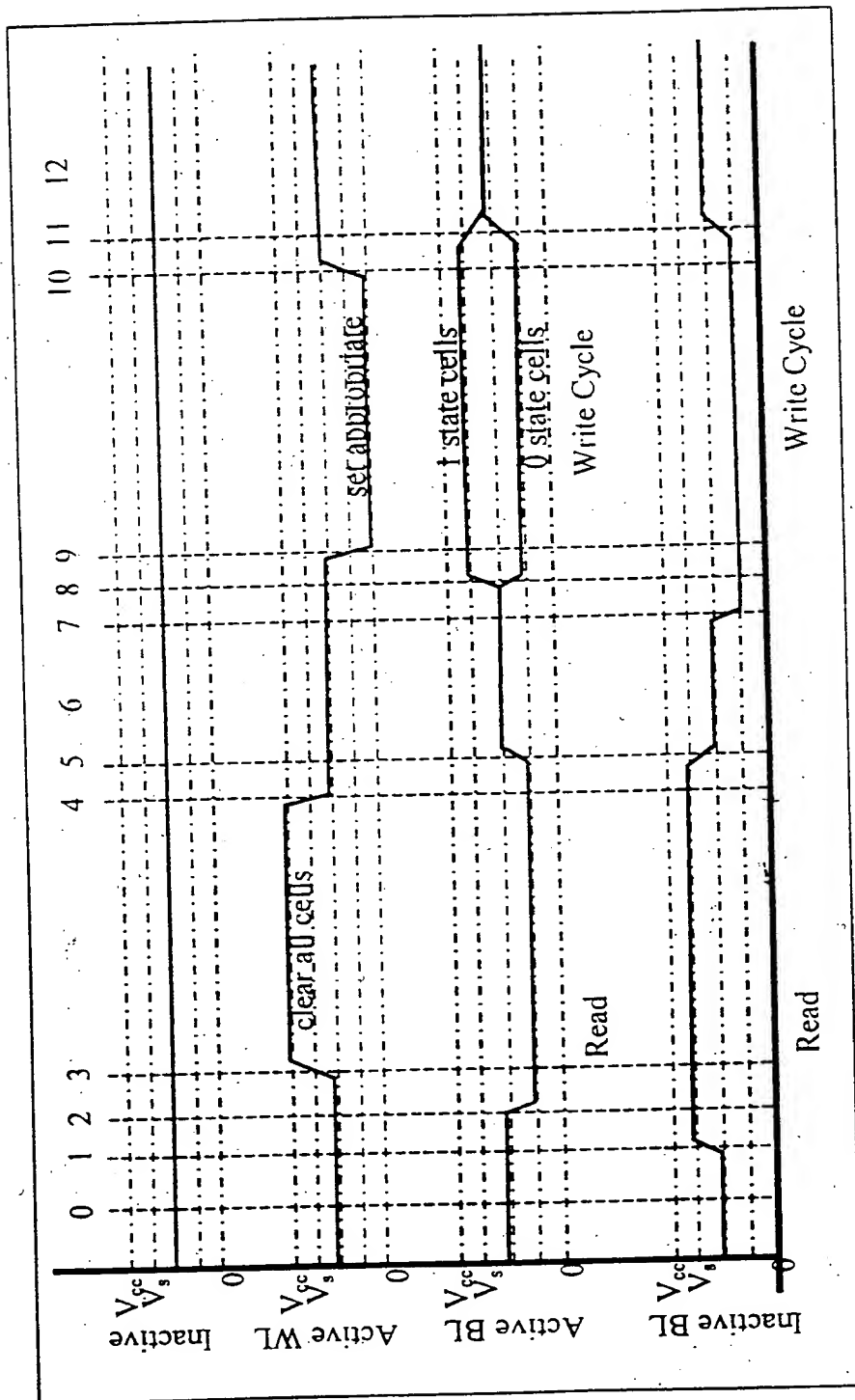


FIG. 9

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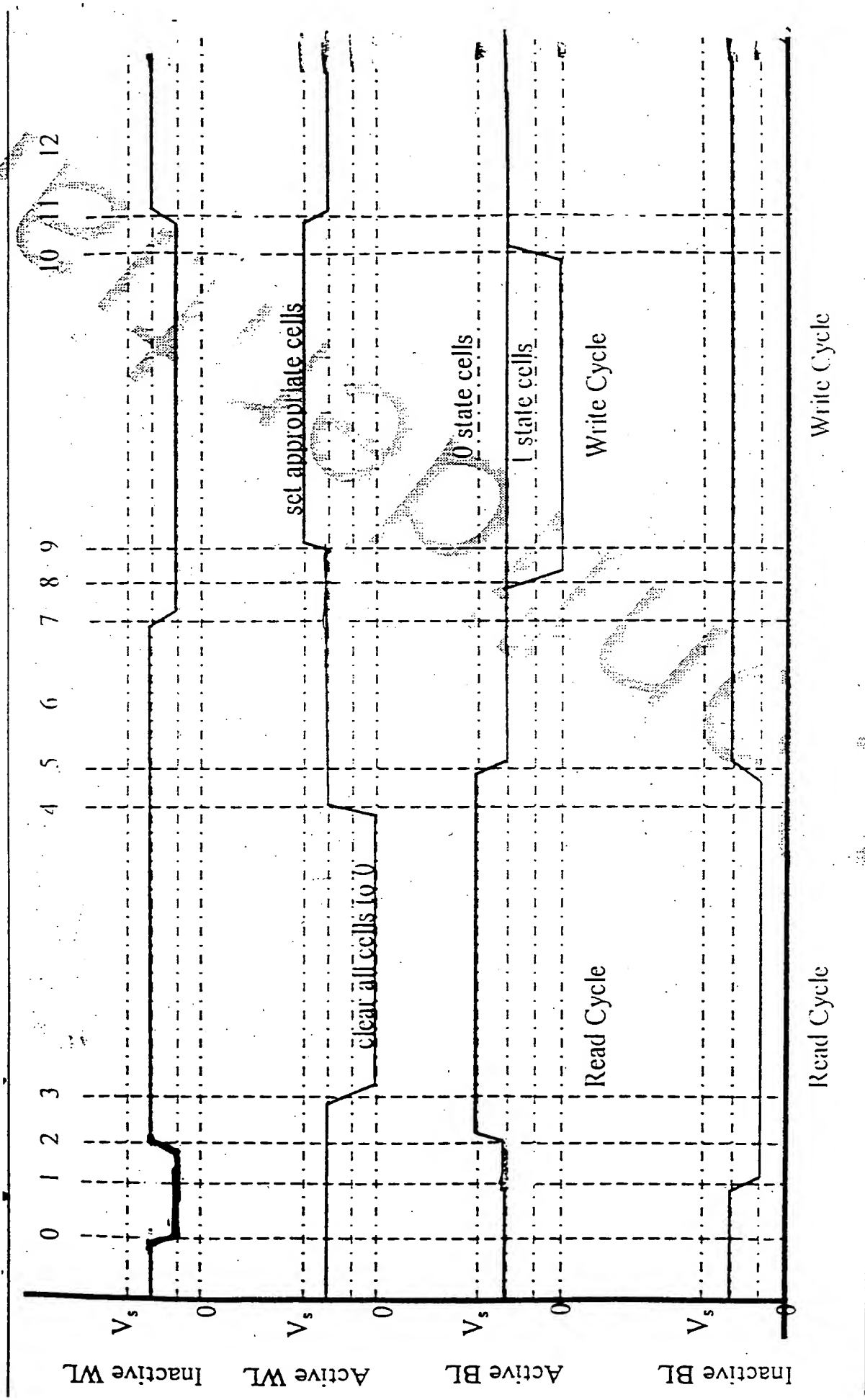


Fig. 10

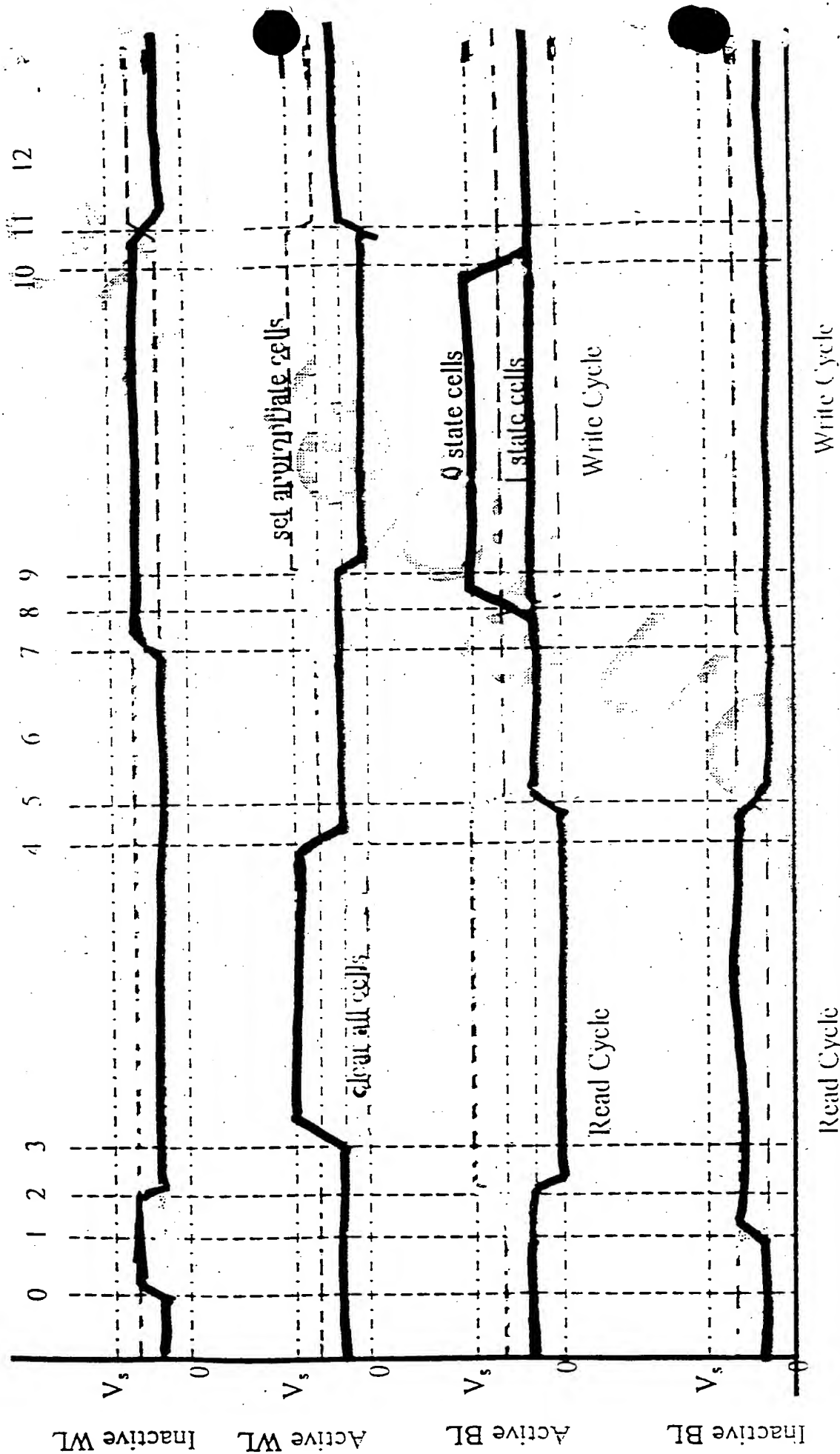


Fig. 11

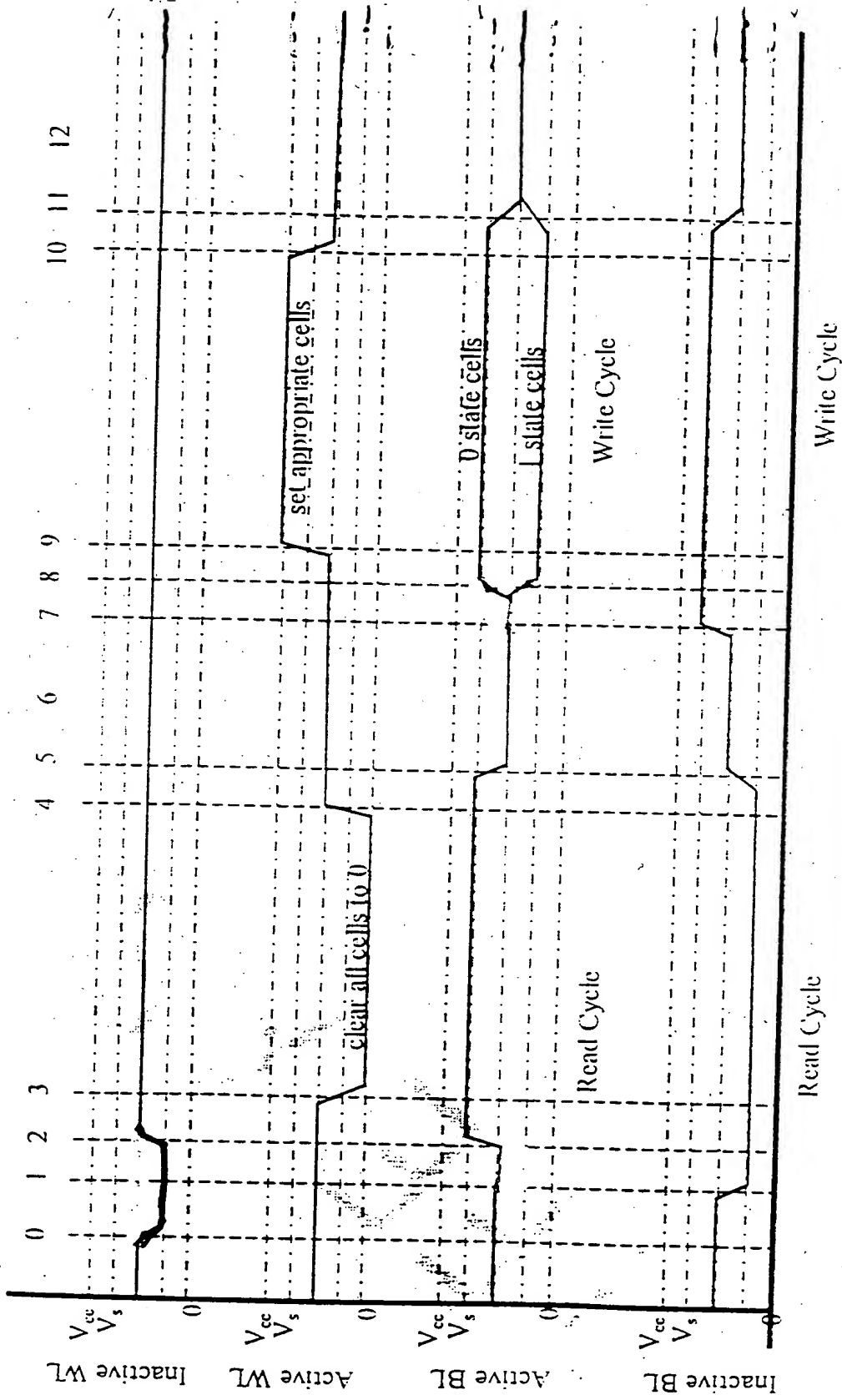
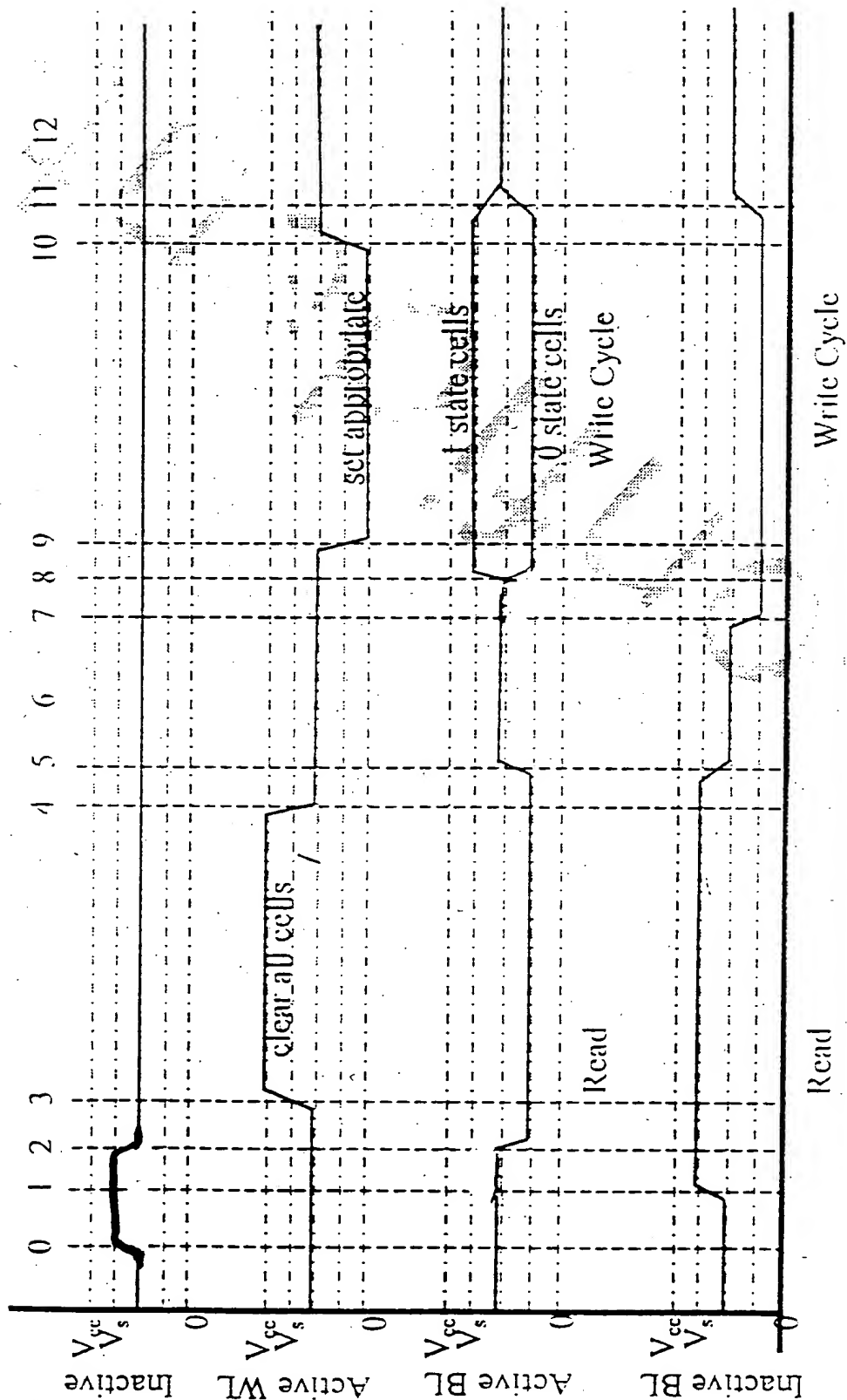


FIG.12



F16.13

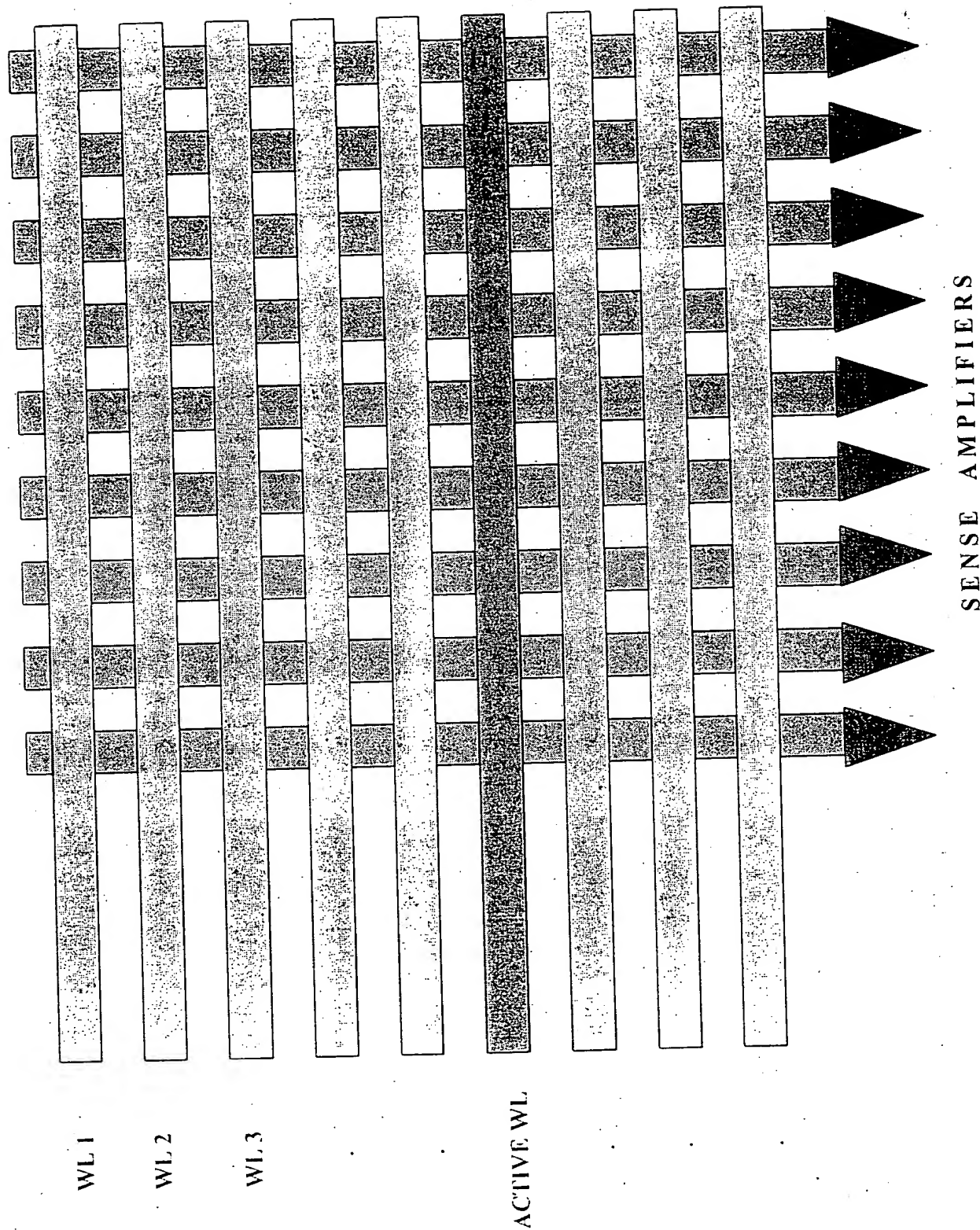


FIG.15